ABSTRACT OF THE DISCLOSURE

The present invention relates to a SDRAM and its control method which write or read data in synchronization with the external clock and its object is to provide a semiconductor memory device and its method which can be easily tested and evaluated by the conventional memory test equipment having a transfer type which transfers the data in synchronization with the rising and falling edges of the external clock. The semiconductor memory device has a write amplifier control section 14 and I/O data buffer/register 22 as a data transfer circuit corresponding to the data transfer type for the DDR type and SDR type. Also, a mode register 28 is formed to be used as a switch signal to switch the data transfer circuit to either DDR type or SDR type.